HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation of application Ser. No. 08/288,685, filed on Aug. 11, 1994, now abandoned, which in turn, is a continuation of application Ser. No. 08/017,511, filed Feb. 12, 1993, now U.S. Pat. No. 5,338,961, which, in turn, is a continuation of application Ser. No. 07/303,818, filed on Jan. 30, 1989 (now U.S. Pat. No. 5,191,396), which, in turn, is a division of application Ser. No. 07/090,664, filed on Aug. 28, 1987 (now abandoned), which, in turn, is a division of application Ser. No. 06/456,813, filed on Jan. 10, 1983 (now U.S. Pat. No. 4,705,759), which, in turn, is a division of application Ser. No. 06/232,713, filed on Feb. 9, 1981 (now U.S. Pat. No. 4,376,286), which is a continuation of application Ser. No. 05/951,310, filed Oct. 13, 1978 (now abandoned).

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specifically relates to a novel structure for a MOSFET device which permits it to be used in high power applications with a relatively high reverse voltage and with an exceptionally low on-resistance. The major advantage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resistance per unit conductive area. The MOSFET transistor has numerous advantages over the bipolar transistor including very high switching speed, very high gain and lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance, its use in high power switching applications has been limited.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device which has a low forward resistance so that the device becomes more competitive with bipolar devices in a switching type application while retaining all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared to the limiting resistance per unit area previously existing in a MOSFET-type device.

In one embodiment of the invention, two sources are placed on the same surface of a semiconductor wafer and are laterally spaced from one another. A gate electrode, deposited on a conventional gate oxide, is disposed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced from one another by an n-type bulk region. Current from each source can flow through its respective channel (after the creation of the inversion layer defining the channel), so that majority carrier conduction current can flow through the bulk region and across the wafer or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally displaced surface region from the source electrodes. This configuration is made using the desirable manufacturing techniques of the D-MOS device which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths. While the above configuration may have been previously described for a MOSFET signal-type device, the structure is not that of the commonly used signal MOSFET.

The device is basically formed in an n(−) substrate which has the relatively high resistivity which is necessary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the n(−) region will have a resistivity of about 20 ohm-centimeters. However, this same necessary high resistivity characteristic has caused the on-resistance of the MOSFET device, when used as a power switch, to be relatively high.

In accordance with the present invention, it has been found that in the upper portion of the central bulk region to which the two inversion layers feed current in the path to the drain electrode, the central region immediately beneath the gate oxide can be a relatively low resistivity material formed, for example, by an n(+) diffusion in that channel region, without affecting the reverse voltage characteristics of the device.

More specifically, and in accordance with the invention, this common channel will have an upper portion beneath the gate oxide and a lower bulk portion extending toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 400 volt device, the lower n(−) region may have a depth of about 35 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be selected, depending on the desired reverse voltage of the device to provide the necessary thicker depletion region required to prevent punch-through during reverse voltage conditions. The upper portion of the common channel is made highly conductive (n+) to a depth of from about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the on-resistance per unit area of the device by more than a factor of two. The resulting device becomes competitive with conventional high power bipolar switching devices since it retains all of the advantages of the MOSFET device over the bipolar device but now has the relatively low forward resistance which was the major characterizing advantage of the bipolar device.

In accordance with another feature of the present invention, the p-type region which defines, the channel beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion region will have a large radius of curvature in the n(−) epitaxial layer forming the body of the device. This deeper diffusion or deeper junction has been found to improve the voltage gradient at the edge of the device and thus permits the use of the device with higher reverse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a high power MOSFET chip which incorporates the present invention and particularly illustrates the metalizing patterns of the two sources and the gate.

FIG. **2** is a cross-sectional view of FIG. **1** taken across the section line **2—2** in FIG. **1**.

FIG. **3** is a cross-sectional view similar to FIG. **2** showing the initial step in the process of manufacture of the chip of FIG. **1** and **2** and particularly shows the p(+) conductivity implant and diffusion step.

FIG. **4** shows the second step in the manufacturing process and shows the n(+) implant and diffusion step.

FIG. **5** shows a further step in the process of manufacture of the chip of FIGS. **1** and **2** and shows the channel implant and diffusion step.

FIG. **6** shows a further step in the process of manufacture and illustrates the source predeposition and diffusion step.